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Specifications and Interfaces

CYAN is a high channel count, ultra wide band, high gain, direct conversion quadrature transceiver[1] and signal processing platform. Providing simultaneous support for up 16, fully independent, transmit or receive radio channels, this flexible platform uses four 40GBASE-R qSFP ports to quickly receive and transmit radio data. With a standard instantaneous bandwidth of 1GHz (upgradable to 3GHz using our high bandwidth option), 16 bit converter resolution, and a tunable RF range between 100kHz to 20GHz, CYAN aims to provide end users with the best possible performance available from a commercial vendor. CYAN is compatible with various signal processing tool kits, including GNU Radio and includes source code for many of its drivers and peripherals.

Absolute Maximum Ratings

Stresses beyond those listed in the Absolute Ratings Table (Table 1.1 on the following page) may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and is, therefore, not recommended.

WARNING
EXCEEDING ABSOLUTE RATINGS MAY DAMAGE DEVICE AND MAY CAUSE DANGEROUS FIRE OR ELECTRICAL HAZARDS
Exceeding these ratings may substantially damage device, and the resulting hazards may cause serious personal injury or death.

[1] CYAN is capable of Digital Down/Up Conversion, so superhet architectures can be implemented using Digital Down/Up Conversion on the FPGA.

Table 1.1: Absolute Ratings: Exposure or sustained operation at absolute ratings may permanently damage Cyan. Ensure fan inlets (located on both sides of the device) are not blocked during operation.

Specifications	Min	Max	Units	Notes
Operating Temperature	5	40	C	At fan inlet
Operating Humidity	5	100	%	Non-Condensing
Storage Temperature	0	40	C	
Storage Humidity	20	95	%	Non-Condensing
Input RF Power		10	dBm	Do not exceed.
IO and TRIG Voltage		1.8	V	Do not exceed: Direct to FPGA.
External Reference		3	Vpp	Do not exceed.
SMA Torque	0.6	0.7	Nm	

Specifications

CYAN is a very flexible radio and signal processing platform that supports high bandwidth communications over a wide tuning range. Specific performance figures are provided as an appendix to this manual; for specific measurements, please contact Per Vices.

To provide a general idea of what this product is capable of, Table 1.2 on the next page lists some conservative figures of its out-of-box performance. Configuration of the product towards a specific application may see some of these figures exceed at the expense of others. For more information, please do not hesitate to contact us at: *solutions@pervices.com*.

Table 1.2: PRE-RELEASE: Calibration Measurements relative to 20 ° C

	Specification		Min	Nom	Max	Units
Common Radio	RF Stage (LMX2595)		0.5		20	GHz
	Baseband Stage		0.1		500	MHz
	Dynamic Range		25		70	dB
	SFDR				65	dB
Receive Radio	RF Input Power			-40		dBm
	Noise Figure, Rx RF St		3.1		7	dB
	Power Gain	Low	15		45	dB
		High	-10		65	dB
	Group Delay (Radio Chain)[1]	Low		TBD		ns
		High		TBD		ns
Radio Channels	Independent Rx/Tx Channels[2]			16		-
(Receive Converter)	ADC resolution[3]		12	16		bits
	ADC Sample Rate [3]			1	3	GSPS
	Rx Sampling Bandwidth			1	3	GHz
	Latency (input to serial)[1]					ns
Receive DSP and FPGA Specifications (Default firmware)	Decimation ($\frac{f_s}{n}$)		1		65534	-
	Latency (FPGA DSP)[1]			TBD		ns
Transmit Radio	Transmit Power	Low	-10		18	dBm
	Group Delay (radio chain)[1]	Low		TBD		ns
		High		TBD		ns
DAC (Transmit Converter)	Tx Output Bandwidth[3]			1		GHz
	DAC resolution			16		bits
	DAC Output Bandwidth			6		GHz
	Latency (serial to output)[1]					ns
Transmit DSP and FPGA Specifications	Interpolation ($n \cdot f_s$)		1		65534	-
	Latency (FPGA DSP)[1]					ns
Digital	FPGA - Stratix 10 SOC			1SX280HU3F50		-
	On Board Processor Core			ARM Cortex-A53		
	HPS RAM (DDR4)			16		Gb
	FPGA RAM (DDR4, x2)			64		Gb
	NAND Flash (x8)			4		Gb
Networking	40GBASE-R, Data[4]	(x4)	each	40		Gbps
	1000BASE-T, Management	(x2)	each	1		Gbps
Int. Reference (10MHz)	Frequency Stability		-5		5	ppb
Ext. Reference (10MHz)	Input Voltage Swing		2.5		3	Vpp
IO, PPS, and TRIG	FPGA IO Voltage Range		0		1.8	V

[1]For additional information on latency, please contact us.
[2]Default product contains 8 Rx and 8 Tx channels, but may be customized to support an arbitrary number of Rx or Tx channels.
[3]Default product contains 1GSPS convertor with 16bit resolution. High bandwidth variant supports 3GSPS converter with 12bit resolution.
[4]Default product contains 8 Rx and 8 Tx channels, but may be customized to support any number of channels on page ??.