Specifications and Interfaces

Crimson TNG is a wide band, high gain, direct conversion quadrature transceiver and signal processing platform. Using analogue and digital conversion, it is capable of processing signal bandwidths up to 325MHz from approximately DC to 6GHz. Crimson TNG is compatible with GNU Radio and includes source code for many of its drivers and peripherals.

As Crimson TNG is capable of Digital Down/Up Conversion, superhet architectures can be implemented using Digital Down/Up Conversion on the FPGA.

Absolute Maximum Ratings

Stresses beyond those listed in the Absolute Ratings table 1 may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and is, therefore, not recommended.

Specification	min	max	units	notes
Operating Temperature	5	40	C	At fan inlet
Operating Humidity	5	100	%	Non-condensing
Storage Temperature	0	40	C	
Storage Humidity	20	95	%	Non-condensing
Input RF Power		15	dBm	

Table 1: Absolute Ratings: Exposure or sustained operation at absolute ratings may permanently damage Crimson TNG. Ensure fan intake vents (located on both sides of the device) are not blocked during operation.

Observed Performance

Crimson TNG is a very flexible radio and signal processing platform that supports high bandwith communications over a wide tuning range. The hardware and signal processing capabilities may be configured to support a very wide variety of applications, each with their own figures of merit. It is, therefore, fairly challenging to provide uniform performance specifications across those different configurations.

To provide a general idea of what this product is capable of, table 2 on page 15 provides some conservative figures of its out-of-box

performance. Configuration of the product towards a specific application may see you exceed some of these figures at the expense of others. For more information, please do not hesitate to contact us.

External Interfaces

CRIMSON TNG has a number of user accessible external interfaces through which the device can connect to external sources and sinks. Management functions are carried out over a web page hosted by the CRIMSON TNG transceiver and accessible using the management Ethernet port on the front face of the device. Data is sent over the 10Gbps SFP+ ports and receive and transmit antennas connect to the SMA connectors on the front of the device. Other peripherals ports provide access or the capability to improve functionality.

10/100 Management Port This connects to a Linux system that is running on the Hard Processing System located on the FPGA silicon, and provides a unified interface by which to control and configure the remaining devices.

10GBASE-R SFP+ There are two SFP+ ports on the front panel of the device that use 10GBASE-R encoding to directly communicate with an optical module and interface with a ten gigabit network. These ports directly interface with the FPGA fabric and support high bandwidth, low latency communication between the ADCs and DACs.

Please note, not all 10Gbps NICs support 10GBASE-R protocols - it is important that you ensure the card you select supports communication using 10GBASE-R. If you have questions about this, please do not hesitate to contact us

50Ω SMA There are a number of standard SMA headers. These are used to connect to external antennas, sinks, or sources, including:

- Rx — The four independent receive channels may be connected to an external source or antenna
- Tx — The four independent transmit channels may be connected to external antennas or sinks
- Ext. Osc — For the most demanding applications, an external oscillator may be used to drive the LMK04828 outputs. This implies a completely external synchronization solution
- Ext. PLL — A reference clock for local oscillator generation for the frequency synthesizers for receive and transmit PCBs
- Ext. Sys — The system reference clock for converter devices and the FPGA; only present when a sysref command is issued

Ext. Dev	An external 322.265625MHz clock directly to the converter devices as well as the FPGA
Ext. Ref	An external 10MHz reference may be applied to this port in lieu of the default, internal, 10MHz reference
Int. Ref	Crimson TNG may be used to output a 10MHz reference clock to other systems
PPS	This port can be used to synchronise internal time keeping (note: this will be enabled in future releases)
TRIG	This port can be used as a trigger (note: this will be enabled in future releases)

USB 2.0 A USB port is provided that connects to the Linux system running on the Hard Processor System.

Micro-SD slot The FPGA and Hard Processor System may be rebooted or configured using an external Micro-SD card.

ICE320 Power A standard «computer» cable plugs into this power to power the unit. The power supply accepts 120V or 240V.

Operating System

Crimson TNG may be used with any operating system. After connecting the Crimson TNG Transceiver to an external network or computer using its dedicated Ethernet management port, you may configure the device using the provided web interface. It is also possible to SSH into the small Linux distribution running on the processor on-board.

Network Interface Card (NIC) Requirements

Crimson TNG uses a 10-gigabit Ethernet connection to quickly send and receive data. The Crimson TNG uses a 10GBASE-R PHY that interfaces with the SFP+ port using a single, 10.3125Gbps serial lane and a scrambled 64B/66B coding scheme. It is very important to ensure that network devices or interfaces intended to be used to connect to Crimson TNG support 10GBASE-R. The 10GBASE-R family includes 10GBASE-KR, 10GBASE-SR, 10GBASE-LR, and 10GBASE-ER interfaces.

Note that Crimson TNG also requires active cabling: using passive, direct connect, SFP+ cables is not supported. We recommend using active optical cabling (AOC) with integrated SFP+ transceivers.

There is a significant difference between a 10GBASE-X interface (4 serial lanes specified to 3.125Gbps using 8b/10b coding), and the 10GBASE-R interface (1 serial lanes specified to 10.3125Gbps using 64b/66b coding) that Crimson TNG uses. Although both standards may expose the same mechanical SFP+ interface (and thereby allowing you to mechanically connect the two

Alternatively, you may also choose to use a fibre cable and a compatible 10GBASE-R SFP+ optical transceiver module.

If you have any questions or concerns about NIC card requirements, please do not hesitate to contact us.

Mechanical

CRIMSON TNG conforms to a 1U form factor and 19-inch+ rack. A mechanical drawing in included in the Appendix.

RF Chain

Simulated RF chain performance (based on component specifications) yield the simulated performance indicated in table 3 on page 16. As both the receive and transmission chains use variable stages, the figures were calculated using midpoint references for attenuation and gain stages. With proper tuning and calibration, you should expect better values. More information on the specific RF chain used may be found in the System Architecture chapter on page 17.

Specification		min	nom	max	units
Common Radio					
RF Stage (ADF4355)		110		6800	MHz
Baseband Stage		0.1		140	MHz
Dyn. Range		25		70	dB
SFDR				65	dB
Receive Radio					
RF Input Power			-20		dBm
Noise Figure, Rx RF St		3.1		7	dB
Power Gain	Low	15		45	dB
	High	-10		65	dB
Group Delay (Radio Chain)	Low		13.7		ns
	High		20		ns
ADC (Receive Converter)					
Independent Channels			4		-
ADC resolution			16		bits
ADC Sample Rate [1]			322.265625	325	MSPS
Rx Sampling Bandwidth			322.265625		MHz
Latency (input to serial)			50		ns
Receive DSP and FPGA Specifications (Default firmware)					
Decimation ($\frac{f_s}{n}$)		1		256	-
Latency (FPGA DSP)		50	500	750	ns
Transmit Radio					
Transmit Power	Low	-30		18	dBm
	High	-10		15	dBm
Group Delay (radio chain)	Low		5		ns
	High		11		ns
DAC (Transmit Converter)					
Tx Output Bandwidth			322.265625		MHz
DAC resolution			16		bits
DAC Sample Rate			322.265625	325	MSPS
Latency (serial to output)		50	655	804	ns
Transmit DSP and FPGA Specifications					
Interpolation ($n \cdot f_s$)		1		256	-
Latency (FPGA DSP)		96		160	ns
Digital					
FPGA - Arria V ST SOC			5ASTMD3E3F31		-
On Board Processor Core			ARM Cortex-A9 MP		
LPDDR2 RAM			4		Gb
NAND Flash (x8)			4		Gb
Networking					
10GBASE-R, Full Duplex	each		8		Gbps
Default IP, SFP+ Port A			10.10.10.2		-
Default IP, SFP+ Port B			10.10.11.2		-
Internal Reference (10 MHz)					
Frequency Calibration		-5		5	ppb

Table 2: Observed Performance. These specifications reference observations taken during internal use and development. Calibration Measurements relative to 20^oC

Specification	Value	units
Input Parameters		
Input Power	-55	dBm
Frequency	2000	MHz
Analysis B/W	150	MHz

Specification	Value		units
Rx Chain Analysis			
	LNA	LNA +PA	
NF	4.8	3.1	dB
SFDR	55	47	dB
IMD	-113	-81	dB
IIP3	-1.3	-17	dBm
SNR	32	33	dB
Rx Sensitivity	-86	-87	dBm
Input P1dB	-28	-44	dBm
Tx Chain Analysis			
Power Gain	-20-5		dBm
SFDR	40-70		dB

Table 3: These specifications are intended to serve as a broad guide, with variable gain and attenuation stages set at mid-points. As variable stages are adjusted, performance generally improves.