Specifications and Interfaces

Crimson is a wide band, high gain, direct conversion quadrature transceiver and signal processing platform. Using analogue and digital conversion, it is capable of processing signal bandwidths up to 322MHz from approximately DC to 6GHz. Crimson is compatible with GnuRadio, and includes source code for many of its drivers and peripherals.

As Crimson is capable of Digital Down/Up Conversion, superhet architectures can be implemented using Digital Down/Up Conversion on the FPGA.

Absolute Maximum Ratings

Stresses beyond those listed in table 1, Absolute Ratings, may cause permanent damage to the device. These ratings are stress specifications only; functional operation of the product at these conditions is not implied - exposure to absolute maximum rating conditions for extended periods of time may affect reliability and is not recommended.

Specification	min	max	units
Operating Temperature	5	85	C
Storage Temperature	0	70	C
Input RF Power		15	dBm

Table 1: Absolute Ratings: Exposure or sustained operation at absolute ratings may permanently damage Crimson. Ensure fan intake vents are not blocked during operation.

Observed Performance

The specifications listed in table 2 on the next page detail observed performance under typical conditions. They are intended as a loose guide to what we have observed during internal testing; please contact us if you require specific specifications.

External Interfaces

Crimson has a number of user accessible external interfaces through which the device can connect to external sources and sinks. Speaking broadly, management functions are generally carried out over a web

Specification	min	nom	max	units
Temperature				
Card Operating Temperature		70		C
Analogue				
RF Tuning (HMC833)	25		6000	MHz
Dyn. Range (RX,TX)	10		70	dB
SFDR (RX, TX)			65	dB
Power Gain (RX, High) @2GHz	-4.5		65	dB
Power Gain (RX, Low) @ 125MHz	-15		+55	dB
Nominal RF Input Power		-20		dBm
Rx, Noise Figure	3.5		11	dB
TX Power @ 10MHz		20		dBm
Digital				
FPGA - Arria V ST SOC	5ASTMD3E3F31			-
On Board Processor Core	ARM Cortex-A9 MP			
LPDDR2 RAM	4			Gb
NAND Flash (x8)	4			Gb
Networking				
10Gbe Data Rate (full duplex)		8		Gbps
Sampling				
ADC resolution		16		bits
ADC Sample Rate (per IQ Channel)		322.265625		MSPS
DAC resolution		16		bits
DAC Sample Rate (per IQ Channel)		322.265625		MSPS
Decimation (2^n), n=[0,5]	0		32	-
Interpolation (2^n), n=[0,5]	0		32	-
Internal Reference (10 MHz)				
Frequency Calibration (20^0C)	-5		5	ppb

Table 2: Observed Performance. These specifications reference observations taken during internal use and development.

page, hosted by the CRIMSON transceiver, and accessible using the gigabit Ethernet port on the front face of the device, and data is sent over the 10Gbps SFP+ ports. Receive and transmit antennas connect to the SMA connectors on the front of the device. Other peripherals ports provide access or the capability to improve functionality.

Gigabit Management Port This connects to a Linux system that is running on the Hard Processing System located on the FPGA silicon, and provides a unified interface by which to control and configure the remaining devices.

10Gbps SFP+ There are two 10Gbps ports on the front panel of the device. These ports support using an SFP+ connector to interface with a ten gigabit network. These ports directly

interface with the FPGA fabric and support high band-width, low latency, communication between the ADCs and DACs.

50Ω SMA There are a number of standard SMA headers, which are used to connect to external antennas, sinks, or sources, including:

Rx The four independent receive channels may be connected to an external source or antenna

Txgit The four independent transmit channels may be connected to external antennas or sinks

Ext. Ref An external 10MHz reference may be applied to this port in lieu of the default, internal, 10MHz reference

Ext. Sync An external sync may be applied to this port to synchronize the time keeping across multiple devices, using the features provided in the LMK04828 chip

Ext. VCO For the most demanding applications, an external VCO may be used to drive the LMK04828 outputs. This implies a completely external synchronization solution

USB 2.0 A USB port is provided that connects to the Linux system running on the Hard Processor System.

Micro-SD slot The FPGA and Hard Processor System may be re-booted or configured using an external Micro-SD card.

Mini-SIM slot A Mini-SIM card may be connected, with its contacts directly interfacing to the FPGA fabric.

ICE320 Power A standard «computer» cable plugs into this power to power the unit. The power supply accepts 120V or 240V.

Operating System

Management of the CRIMSON Transceiver occurs using a web inter-face over the management port. It is also possible to SSH into the small Linux distribution running on the processor on-board.

Mechanical

CRIMSON conforms to a 1U form factor and 19-inch+ rack. A me-chanical drawing in included in the Appendix.

RF Chain

Simulated RF chain performance, based on component specifications, yield the simulated performance indicated in table 3. As both the receive and transmission chains use variable stages the figures were calculated using midpoint references for attenuation and gain stages - with proper tuning and calibration, you should expect better values. More information on the specific RF chain used may be found in the System Architecture chapter on the next page.

Specification	Value	units
Input Parameters		
Input Power	-55	dBm
Frequency	2000	MHz
Analysis B/W	150	MHz

Specification	Value	units
Rx Chain Analysis		
SFDR	40-55	dB
IMD	-69	dB
IIP3	-23.5	dB
SNR	33.8	dB
Rx Sensitivity	-85	dBm
Input P1dB	-43	dBm
Tx Chain Analysis		
Power Gain		dB
SFDR		dB

Table 3: These specifications are intended to serve as a broad guide, with variable gain and attenuation stages set at midpoints. As variable stages are adjusted, performance generally improves.